IN THE CLAIMS

Presented below are the amended claims in a clean, un-marked format. For the Examiner's convenience, a copy of all of the claims is included herewith. Amended claims are marked (Amended), while unamended claims are marked (Original), and new claims are marked (Original).

1. (Previously Amended) A method of using a multi-master system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

controlling the multi-master system bus for configuration using a first device, the first device comprising a selectable one of an on-chip central processing unit (CPU), a direct memory access (DMA) controller, and an external control device;

configuring a memory cell in the CSL using the multi-master system bus; and

reading the memory cell in the CSL using the multi-master system bus.

14. (Original) The method of claim 1 further comprising:

mapping the memory cell in the CSL into an addressable memory space of the system bus.

15. (Original) The method of claim 14 wherein reading a memory cell in the CSL using the system bus is performed by a second device selected from the group consisting of the CPU, the direct memory access (DMA) controller, and the external control device.

16. (Original) The method of claim 15 further comprising:

mapping a random access memory (RAM) cell in the CSoC into the addressable memory space of the system bus.

17. (Original) The method of claim 16 further comprising:

reading the RAM cell using the system bus.

18. (Original) The method of claim 17 wherein reading the RAM cell using the system bus is performed by a third device selected from the group consisting of the CPU, the direct memory access (DMA) controller, and the external control device.

19. (Original) The method of claim 1 wherein the system bus is used for configuration and general interconnect.

20. (Original) The method of claim 19 further comprising:

selecting a signal with a multiplexer in the CSoC to determine if the system bus is used for configuration or general interconnect.

21. (Previously Amended) A method of configuring a configurable system on a chip (CsoC) comprising:

initiating configuration of the CsoC using an on-chip central processing unit (CPU);

passing control of a multi-master system bus to a first device for configuring on-chip configurable system logic (CSL);

configuring a memory cell in the CSL using the first device.

22. (Original) The method of claim 21, wherein the first device is selected from a group consisting of the CPU, a direct memory access (DMA) controller, and an external control device.

23. (Original) The method of claim 21 further comprising:

reading a memory cell in the CSL using a second device selected from a group consisting of the CPU, a direct memory access (DMA) controller, and an external control device.

24. (Original) The method of claim 21 further comprising:

mapping the memory cell in the CSL into an addressable memory space of the system bus.

25. (Original) The method of claim 24 further comprising:

mapping a random access memory (RAM) cell in the CSoC into the addressable memory space of the system bus.

26. (Original) The method of claim 25 further comprising:

reading the RAM cell using the system bus.

27. (Original) The method of claim 26, wherein reading the RAM cell using the system bus is performed by a third device selected from the group consisting of the CPU, a direct memory access (DMA) controller, and an external control device.

28. (Original) The method of claim 21 wherein the system bus is used for configuration and general interconnect of the CSoC.

29. (Original) The method of claim 28 further comprising:

selecting a signal in the CSoC to indicate that the system bus is being used for configuration rather than general interconnect of the CSoC.

30. (Original) A method comprising:

initiating configuration of a configurable system on chip (CsoC) using an on-chip central processing unit (CPU);

configuring a memory cell in the CSL using a first device of a group of devices, the group of devices comprising the CPU, a direct memory access (DMA) controller, and an external control device;

reading a memory cell in the CSL using a second device selected from the group of devices; and

selecting a signal in the CSoC to determine if the system bus is used for configuration or general interconnect of the CSoC.

31. (Original) The method of claim 30, wherein the first device and the second device are the same device.

32. (Original) The method of claim 30, wherein control of a system bus on the CSoC is by the on-chip CPU, the first device, or the second device based on which device is performing operations on the CSL.